

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	203	instruction adj set adj simulator	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 15:57
L2	14	1 and microcontroller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:51
L3	5806	microcontroller and simulat\$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:52
L4	60	microcontroller and simulation.ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:52
L5	6	4 and ((test adj bench) or stimulus)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:55
L6	0	("8051" adj3 simulation) and markers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:56
L7	1	("8051" same simulation) and markers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 16:56
L8	6	(microcontroller same simulation) and markers	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/16 17:46
L9	361	(703/22).CCLS.	USPAT	OR	OFF	2005/06/16 17:46

L10	8	9 and microcontroller	USPAT	OR	OFF	2005/06/16 17:48
L11	7	10 and clock	USPAT	OR	OFF	2005/06/16 17:48
L12	11	("5103394" "5604895" "5613098" "5671352" "5680584" "5745767").PN. OR ("6223144").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/16 17:49

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Found microcontroller within 1 word of simulation (+ instruction set simulator). First 16 results of about 58 from 2 queries.

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29K Family Microcontroller Architecture Simulation. Simulator Command-Line ...

instruction set simulator isstip and the architectural **simulator** sim29. ...

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The 68HC812A4 **microcontroller simulation** can run in Expanded Wide, ... The COP

timer, internal RAM and EEPROM, and the full **instruction set** are implemented. ...

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The MC9S12DP256B **microcontroller simulation** runs in Single Chip modes. ...

Instruction timing is emulated. The 68HCS12 **simulator** will run Motorola's D-Bug12 ...

<http://www.aimy.us/68hcs12.html> - 6k - Cached - Similar pages

Advanced Microcontroller Interfacing Laboratory [distance: 0]

A microcontroller course using a **simulator-based lab** would be restricted to ...

What is needed to **set up** an Advanced Microcontroller Laboratory is a ...

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E245SYLc.DOC [distance: 0]

Mentor Graphics ModelSim **Simulator**, f. Back-end implementation tools (Xilinx)

Place and ... Basic parts of a Computer: ISA (**Instruction Set Architecture**), ...

http://www.connix.com/~reed/class/SYL_CR246_04.doc - - Cached - Similar pages

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Microelectronics, 1999. ICM '99. The Eleventh International Conference on 22-24 Nov. 1999 Page(s):177 - 180

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Design, Automation and Test in Europe Conference and Exhibition 2000. Proceedings 27-30 March 2000 Page(s):742

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Elias, N.J.;

Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE Volume 2, 9-13 Feb. 2003 Page(s):996 - 1001 vol.2

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Wick, C.E.;

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Sim, J.D.; Galbraith, F.S.; Davenport, N.;

Electromagnetic Compatibility, 1997. 10th International Conference on (Conf. Publ. No. 445) 1-3 Sept. 1997 Page(s):100 - 104

[AbstractPlus](#) | Full Text: [PDF\(492 KB\)](#) IEEE CNF**7. UV151: a simulation tool for teaching/learning the 8051 microcontroller**

del Rio, A.; Andina, J.J.R.;

Frontiers in Education Conference., 2000. FIE 2000. 30th Annual Volume 2, 18-21 Oct. 2000 Page(s):F4E/11 - F4E/16 vol.2

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Published before September 1998

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Gearold R. Johnson, Robert A. Mueller

March 1976 **ACM SIGPLAN Notices , Proceedings of the ACM SIGMINI/SIGPLAN interface meeting on Programming systems in the small processor environment**, Volume 11 Issue 4

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ASM/GEN and SIM/GEN are a software system comprised of a set of independent FORTRAN program writer modules designed to generate micro computer and small minicomputer assemblers and simulators. It is simple enough to be used by those with limited architecture and programming backgrounds, but flexible and powerful enough to generate efficient and well-structured assemblers and simulators for small micro/mini computers with sophisticated architectures and instruction sets. This paper presents ...

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Mark D. Aagaard, Robert B. Jones, Carl-Johan H. Seger

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

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We describe the verification of the IM: a large, complex (12,000gates and 1100 latches) circuit that detects and marks the boundaries between Intel architecture (IA-32) instructions. We verified agate-level model of the IM against an implementation-independent specification of IA-32 instruction lengths. We used theorem proving to derive 56 model-checking runs and to verify that the model-checking runs imply that the IM meets the specification for all possible sequences of IA-32 instructions. Our v ...

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